APPLICATION NOTE

TJA1040
CAN High-Speed Transceiver

AN10211

Philips
Semiconductors

PHILIPS

Abstract

The TJA1040 is an advanced CAN High-Speed Transceiver for use in automotive and general industrial applications. It supports the differential bus signal representation being described in the international standard for in-vehicle CAN High-Speed applications (ISO11898). CAN (Controller Area Network) is the standard protocol for serial in-vehicle bus communication, particularly for Engine Management and Body Multiplexing.

The TJA1040 provides a Standby Mode, as known from its functional predecessors PCA82C250 and PCA82C251, though with significantly reduced power consumption. Besides the excellent low-power behaviour the TJA1040 offers several valuable system improvements. Highlights are the absolute passive bus behaviour in case the device is unpowered as well as the excellent EMC performance.

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Summary

This application note provides information on using the TJA1040 within automotive and industrial applications. The functional behaviour of the TJA1040 is described in detail, illustrating the use of the outstanding device characteristics. Several topics of interest like operation modes, hardware application and bus network aspects are discussed. Furthermore the interoperability with the CAN High-Speed Transceivers PCA82C250/C251, TJA1041 and TJA1050 from Philips Semiconductors is considered.

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1. Introduction

The CAN High-Speed Transceiver TJA1040 [1] from Philips Semiconductors provides the physical link between the protocol controller and the physical transmission medium according to ISO11898 [2] and SAE J2284 [3]. This ensures interoperability with other ISO11898 compliant transceiver products.

Since the TJA1040 is based on the same technology as the CAN High-Speed Transceiver TJA1050 [4] it is processed in the advanced Silicon-on-Insulator (SOI) technology. Compared to its functional predecessors PCA82C250 (C250) [5] and PCA82C251 (C251) [6] the TJA1040 shows an reduction of about 20dB in electromagnetic emission (EME). Additionally the electromagnetic immunity (EMI) has improved significantly.

Besides electromagnetic compatibility (EMC), another key feature of the TJA1040 is its Standby Mode. This mode provides a very low current consumption (less than 15μA) and remote wake-up capability via the CAN bus lines using a differential wake-up receiver. This makes the TJA1040 the preferred transceiver for applications, which keep the microcontroller and the applications V_{CC} always active. Moreover the TJA1040 offers ideal passive behaviour when unpowered. It is therefore completely invisible to the bus if the V_{CC} supply of the transceiver is switched off. This feature is of main interest for ignition key controlled nodes (clamp-15), which are unpowered completely when the ignition key is turned off while other ECUs continue communication (partial networking).

The TJA1040 is available without packaging (bare die) as well as in SO8 package as shown in Figure 1-1. It is pin compatible to other CAN High-Speed Transceivers from Philips Semiconductors like the C250, C251 and TJA1050 and the TJA1041 [7] with the upper part of its SO14 pinning.

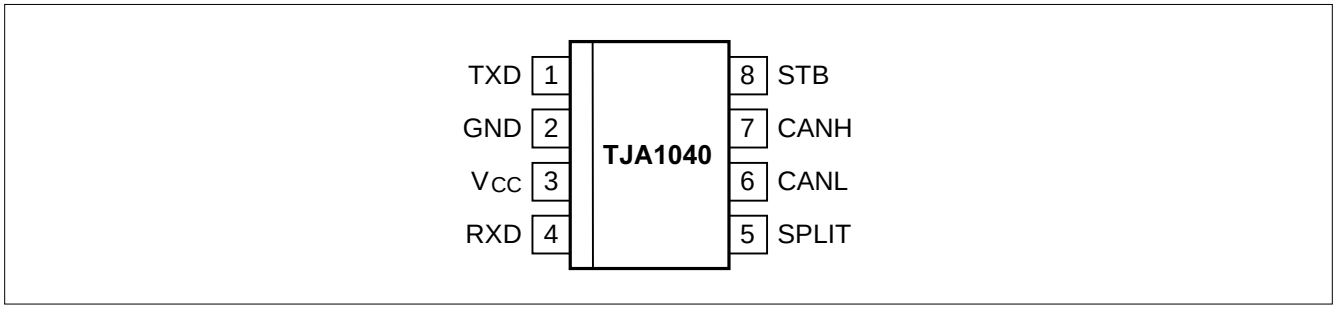

Figure 1-1 : Pinning diagram of the TJA1040

2. General Application of CAN High-Speed

Figure 2-1 illustrates in the bottom a general application of CAN High-Speed. Several ECUs (Electronic Control Units) are connected via stubs to a linear bus topology. Each bus end is terminated with 120Ω (R_T), resulting in the nominal 60Ω busload according to ISO11898. Figure 2-1 shows the split termination concept, which is helpful in improving the EMC of CAN High-Speed bus systems [8]. The former single 120Ω termination resistor is split into two resistors of half value ($R_T/2$) with the center tap connected to ground via the capacitor C_{spl}.

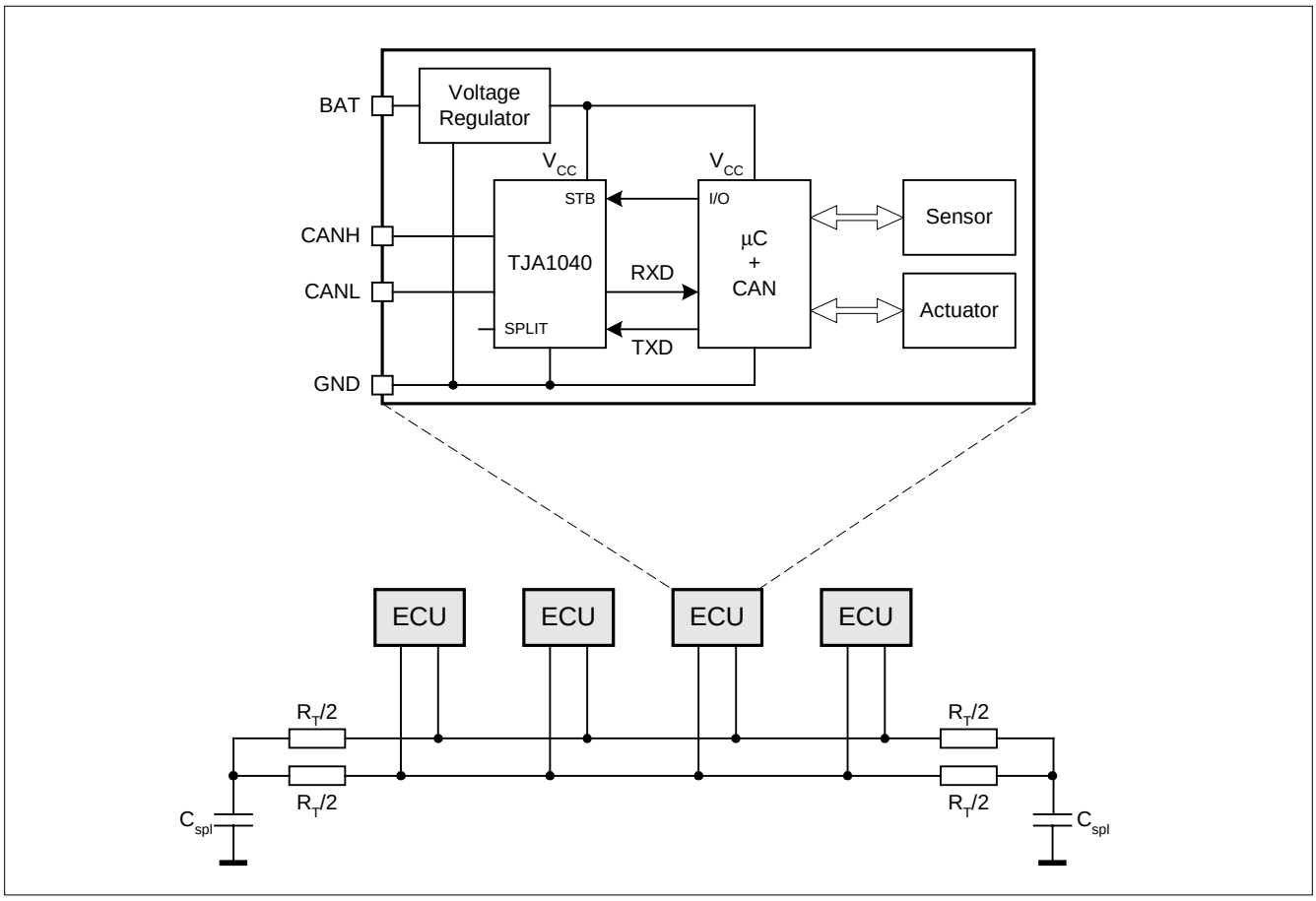

Figure 2-1: Application of CAN High-Speed

The block diagram in the top of Figure 2-1 describes the internal structure of an ECU. Typically an ECU consists of a standalone transceiver (here TJA1040) and a host microcontroller with integrated CAN-controller, which are supplied by a voltage regulator. While the CAN High-Speed Transceiver needs a +5V supply in order to support the ISO11898 bus levels, new microcontroller products are increasingly using lower supply voltages like 3.3V. In this case a dedicated 3.3V voltage regulator is necessary for the microcontroller. The protocol controller is connected to the transceiver via a serial data output line (TXD) and a serial data input line (RXD). The transceiver is attached to the bus lines via its two bus terminals CANH and CANL, which provide differential receive and transmit capability. In case of the TJA1040 the pin STB is connected to an I/O pin of the host microcontroller for operation mode control. The split termination approach can be further improved using the pin SPLIT for DC stabilization of the common mode voltage (see also chapter 4.4).

The protocol controller outputs a serial transmit data stream to the TXD input of the transceiver. An internal pull-up function within the TJA1040 sets the TXD input to logic "HIGH" i.e. the bus output driver stays recessive in case of TXD open circuit condition. In the so-called recessive state (see Figure 2-2) the CANH and CANL pins are biased to a voltage level of $V_{CC}/2$. In case a logic "LOW" level is applied to TXD, the output stage is

activated, thus generating a so-called dominant state on the bus line (Figure 2-2). The output driver CANH provides a source output from V_{CC} and the output driver CANL a sink output towards GND. This is illustrated in Figure 2-3 showing the block diagram of the TJA1040.

If no bus node transmits a dominant bit, the bus stays in recessive state. If one or multiple bus nodes transmit a dominant bit, then the bus lines enter the dominant state thus overriding the recessive state (wired-AND characteristic).

The receiver converts the differential bus signal to a logic level signal, which is output at RXD. The serial receive data stream is provided to the bus protocol controller for decoding. The internal receiver comparator is always active i.e. it monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit-by-bit arbitration scheme of CAN.

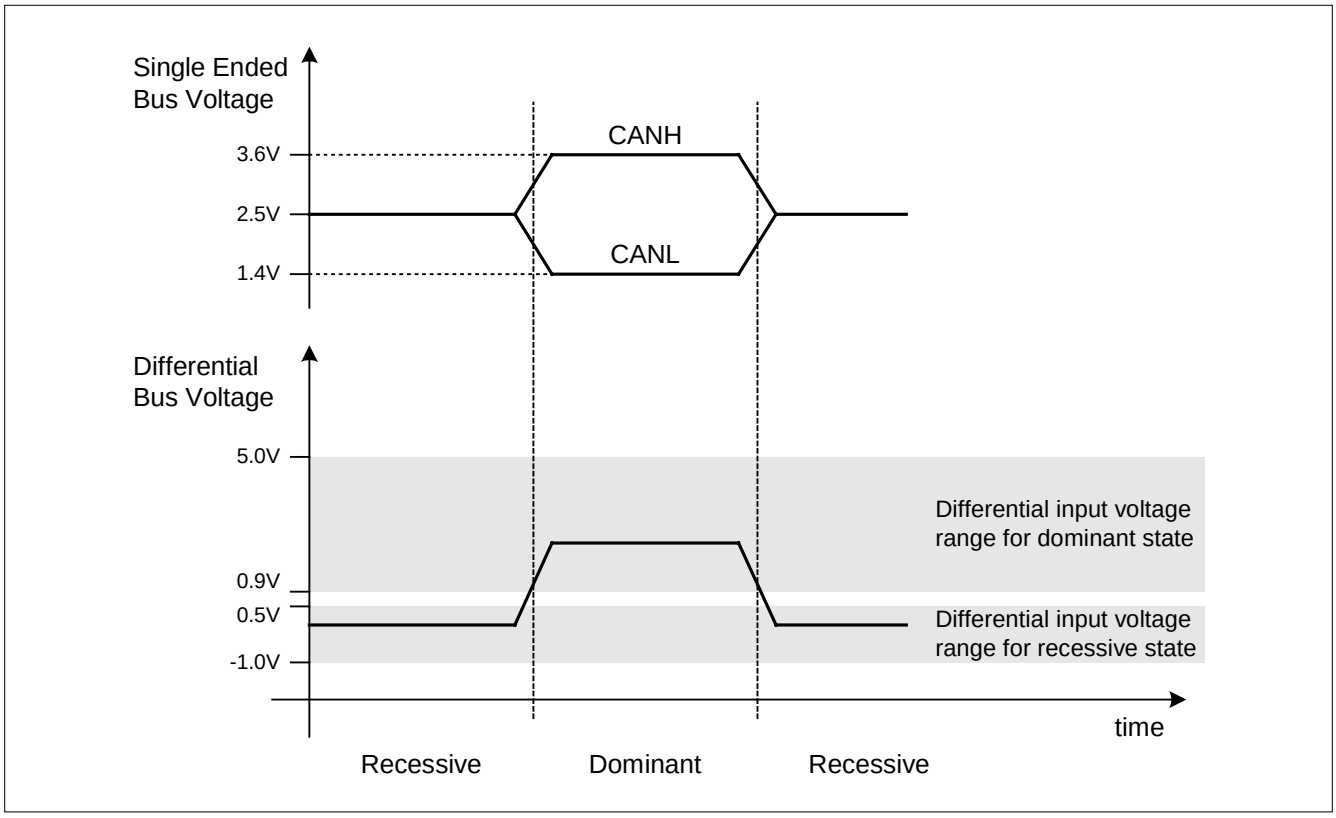

Figure 2-2: Nominal bus levels according to ISO11898

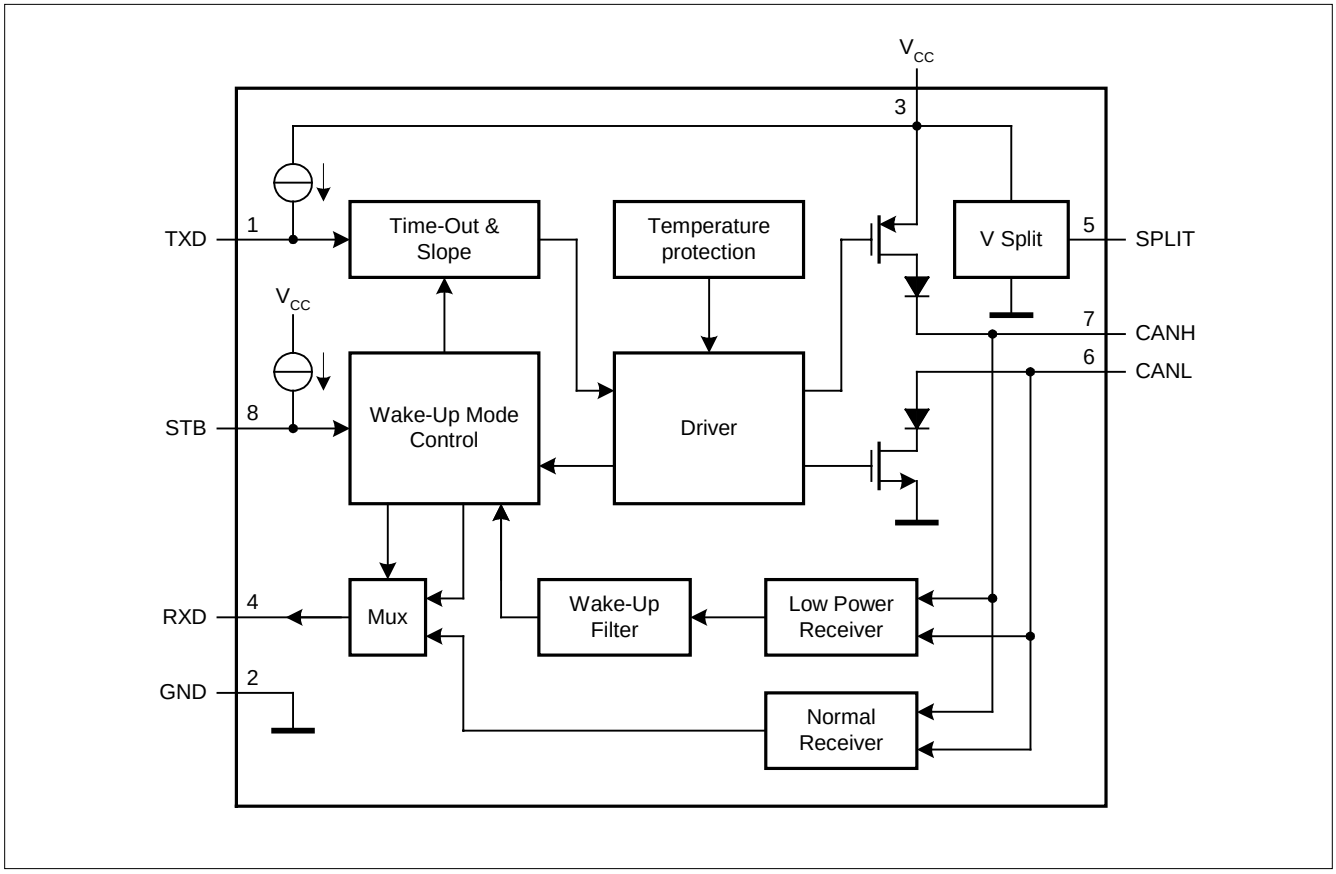

Figure 2-3: Block diagram of the TJA1040

3. Application specific requirements on CAN High-Speed

In-vehicle CAN High-Speed networks come with different requirements, depending on the implemented application. First of all, CAN High-Speed is the ideal choice for all applications, which require a high data throughput (up to 1 Mbit/s). Though from the ECUs power management point of view four different application areas (Type A - D) for CAN High-Speed can be distinguished as illustrated in Figure 3-1.

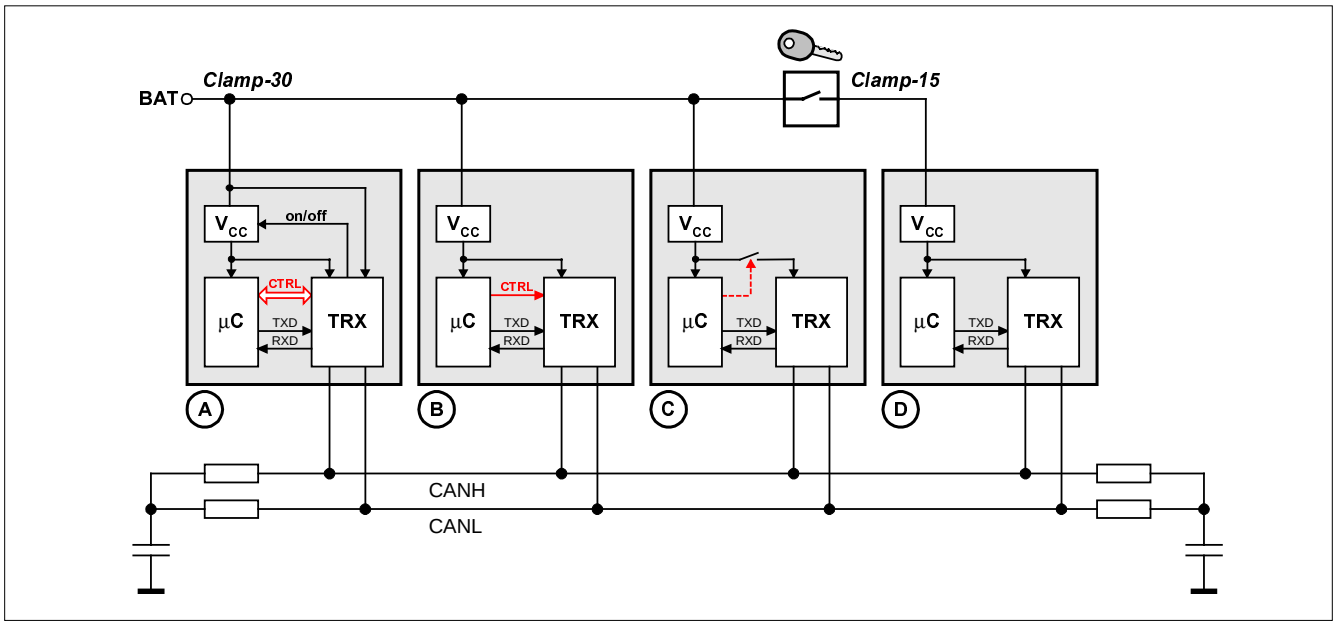

Figure 3-1: Different application areas for CAN High-Speed

A. Applications, which have to be available all time, even when the car is parked and ignition-key is off, are permanently supplied from a permanent battery supply line, often called “Clamp-30”. However, those nodes need the possibility to reduce the current consumption for saving the battery by control of the local ECU supply (V_{CC}). These type-A applications allow switching off the entire supply system of the ECU including the microcontroller supply while keeping the wake-up capability via CAN possible.

B. Those nodes of applications, which need an always-active microcontroller, are permanently supplied from the permanent battery supply line “Clamp-30” using a continuously active V_{CC} supply. In order to reduce the ECUs power consumption, the transceiver needs to be set into a mode with reduced supply current while the V_{CC} stays active.

C. Dedicated applications, which need an always-active microcontroller and therefore are permanently supplied from the "Clamp-30" line, additionally come with a microcontroller controlled transceiver voltage supply. In contrast to type-B applications, further current can be saved, because the transceiver becomes completely unpowered by microcontroller control. These applications require absolute passive bus behaviour of the transceiver, while its voltage supply is inactive. This is needed in order not to affect the remaining bus system, which might still continue communication.

D. Applications, which do not need to be available with ignition-key off, are simply switched off and become totally unpowered during ignition-key off. They are supplied from a switched battery supply line, often called “Clamp-15”. This supply line is only switched on with ignition-key on. Depending on system requirements, e.g. partial communication of the still supplied nodes during “ignition-key off”, these unpowered nodes need to behave passive towards the remaining bus, similar to type-C applications.

The Philips Semiconductors transceiver products TJA1040, TJA1041 and TJA1050 (see also Appendix 11.1) offer different features to completely cover the required power management behaviour.

3.1 Type-A applications

The TJA1041 can be put into a so-called Sleep Mode (all V_{CC} supplies off), which allows reducing the total current consumption of the entire ECU down to typically 20µA, while keeping the capability to receive wake-up events from the bus and to restart the application. The TJA1041 is able to take control over the ECU internal power supply and wake-up requests. It is the first choice transceiver for applications of type A, which need to be remotely available all time.

3.2 Type-B applications

Type-B applications require a dedicated transceiver operation mode with reduced current consumption, while V_{CC} stays active all time. Here the Standby Mode of the TJA1040 offers the best choice for these applications. During Standby Mode the device reduces the V_{CC} supply current to a minimum, in order to save current. In spite of the very low current consumption, the TJA1040 still monitors the CAN bus lines for bus traffic and allows to wake-up the host microcontroller, if desired.

3.3 Type-C and D applications

Within these applications, the supply voltage of the transceiver is directly controlled by the host microcontroller or the ignition key. Thus, the transceiver does not necessarily need to provide a dedicated mode with reduced power consumption. Most important is a passive behaviour of the transceiver, if it becomes unpowered. Parasitic currents within the ECU towards the microcontroller as well as towards the bus lines have to be avoided. Depending on the systems CAN bus requirements, the TJA1040 as well as the TJA1050 are supporting this kind of application.

If there is further bus communication of other CAN ECUs present, while the type-C application transceiver is switched off (partial networking), the TJA1040 offers the first choice. This is, because of its perfectly floating behaviour on the bus lines while V_{CC} is off. So, the remaining bus system keeps unaffected by unpowered TJA1040s.

In case there is no ongoing communication (no partial networking), the TJA1050 offers a comparable alternative. In contrast to the TJA1040, the unpowered TJA1050 would affect the running bus communication due to a small reverse bus current. This would slightly increase the electromagnetic emission during the partial networking time. So, in case there is no ongoing communication, the TJA1050 achieves the same performance like the TJA1040.

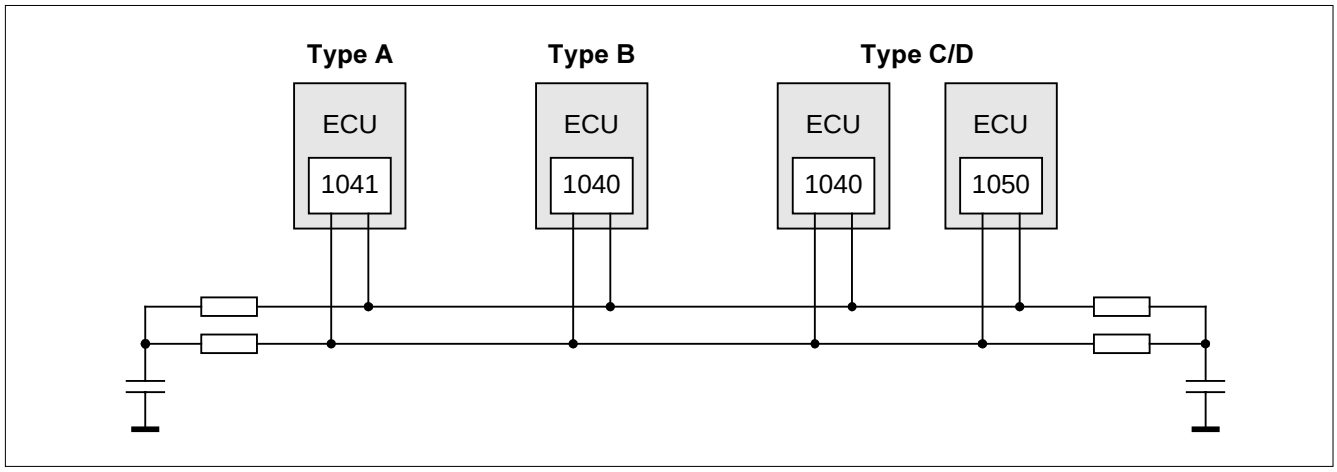

Figure 3-2: Application areas for the TJA1040, TJA1041 and TJA1050

4. Main features of the TJA1040

4.1 Operation Modes

The TJA1040 provides two different operation modes, the Normal Mode and the Standby Mode. Similar to the C250 and C251 transceivers, a dedicated pin selects the actual mode of operation.

4.1.1 Normal Mode

During normal CAN communication the Normal Mode is chosen applying a "LOW" level to the pin STB of the TJA1040. Here the transceiver is able to transmit and receive data via the bus lines CANH and CANL. The digital bit stream input at TXD is transferred into the corresponding analog bus signals. Simultaneously, the "Normal Receiver" (see Figure 2-3) converts the analog data on the bus lines into a digital bit stream, which is output to RXD via the internal multiplexer. In Normal Mode the bus lines are biased to $V_{CC}/2$ and the transmitter is enabled.

4.1.2 Standby Mode

The Standby Mode with significantly reduced current consumption is activated with a “HIGH” level applied to the pin STB. In Standby Mode the transmitter and receiver of the TJA1040 are switched off and therefore the TJA1040 is not capable of transmitting and receiving regular CAN messages. However, a "Low Power Receiver" (see Figure 2-3) monitors the bus lines for CAN messages. Only CAN state changes, which are stable longer than the time t_{BUS} [1] are reflected to the pin RXD and therefore a maximum electromagnetic immunity against unwanted wake-up events is provided. Consequently whenever a dominant phase of longer than t_{BUS} [1] is detected on the bus indicating bus traffic, the RXD pin will become "LOW" (wake-up detected). To enter the Normal Mode after the wake-up detection a "LOW" level has to be applied to the pin STB for activating the "Normal Receiver" of the TJA1040.

Operation Mode	STB	Bus Bias	RXD information	
			RXD = LOW	RXD = HIGH
Normal	LOW	$V_{CC}/2$	Bus dominant	Bus recessive
Standby	HIGH	Ground	Wake-up detected	No wake-up detected

Table 4-1: Operation Modes of the TJA1040

4.2 Excellent EMC behaviour

Electromagnetic compatibility has been one main design target of the TJA1040. During Normal Mode a precondition for a low electromagnetic emission in the critical AM-band is a very good symmetry of the signals CANH and CANL, when switching between the levels dominant and recessive and vice versa. In the TJA1040 design, this symmetry is optimised by using a fixed slope function instead of a variable one, known from the C250/C251. Based on the fixed and optimized slope time, the emission of the TJA1040 could be decreased by more than 20dB compared to the C250/C251, especially if the split termination approach is used. If a specific system implementation needs further reduction of the emission and enhancement of immunity in the FM-band, it is still possible to externally add a common mode choke to the bus pins CANH and CANL.

4.3 Passive behaviour

In nowadays in-vehicle networks typically the so-called partial networking is widely implemented. In chapter 3 partial networking is introduced with different applications. In these typical example applications, some transceivers can become unpowered (e.g. Clamp-15 nodes) while other transceivers are continuously supplied (e.g. Clamp-30 nodes). In such networks the TJA1040 is favoured for those applications, which are partly unpowered, because of its excellent passive behaviour to the bus, when the V_{CC} supply is switched off. Further on the TJA1040 is protected against reverse currents via the pins TXD, RXD and STB if the accompanying microcontroller is still supplied and probably provides a backward supply via those pins.

4.4 Common Mode Stabilization, SPLIT Pin

The high impedance characteristic of the bus during recessive state makes the bus vulnerable to the presence of even small leakage currents, which may occur in case of unpowered transceivers or ECUs within the bus system. As a result the common mode voltage can show a significant voltage drop from the nominal $V_{CC}/2$ value. Upon subsequent transmitting of the first dominant bit of a CAN-message (Start-of-Frame Bit) the common mode voltage would restore to its nominal value, leading to a large common mode step and thus increasing emission. The TJA1040 provides means for common mode stabilization by offering a voltage source of nominal $V_{CC}/2$ at the pin SPLIT (Figure 4-1). In fact the common mode stabilization of the TJA1040 significantly improves the EMC performance even if there are unpowered transceivers with leakage currents connected to the bus.

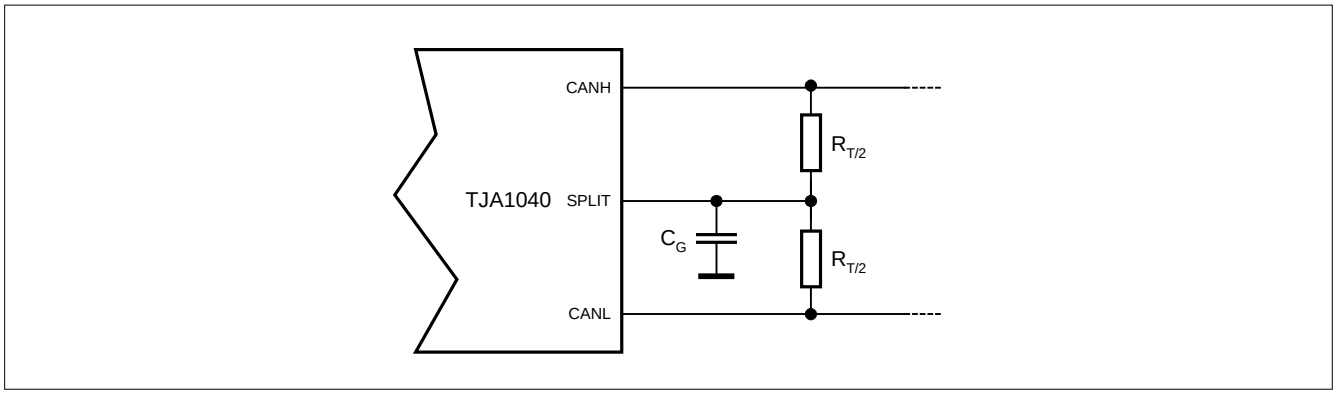

Figure 4-1: Common Mode Stabilization with SPLIT pin

4.5 Interfacing to microcontroller with non 5V supply

As the TJA1040 supports the physical layer of the ISO11898 standard, it requires a +5V supply voltage as reference voltage. On the other hand, new microcontroller generations often require supply voltages lower than 5V, mostly +3.3V and less.

In order to support microcontroller with low supply voltages, the TJA1040 provides a reduced input threshold voltage at its input pins TXD and STB. An input voltage of 2V at these pins is safely interpreted as a “HIGH” level and thus allows a direct drive out of 3V microcontroller. It should be noticed that the output level of the TJA1040’s pins towards the microcontroller is still based on the 5V transceiver supply. TXD and STB are providing an internal weak pull-up current source towards V_{CC} (fail-safe open circuit behaviour) while RXD offers a push-pull driver stage, which drives the pin to V_{CC} in a recessive bus state.

Common 3V microcontroller tolerate voltages above their own supply voltage in case the current is limited. Due to the weak and current limited pull-up source within TXD and STB, a direct connection between the 3V microcontroller and the 5V TJA1040 typically is possible without further protection measures (please check within data sheet of the used microcontroller). Since RXD offers a strong driver towards V_{CC}, the RXD input of the used microcontroller needs to be 5V-tolerant. Alternatively a level shifter or a simple series resistor between RXD of the TJA1040 and the microcontroller could be used.

Please take into account that any hardware between the transceiver's TXD/RXD interface and the microcontroller might lengthen the loop delay of the system, which has an impact on the overall bit timing parameters. Especially at very high bit rates ≥ 500kBit/s, this parameter has to be checked carefully.

4.6 TXD dominant time-out function

The TJA1040 provides the TXD dominant time-out function, which prevents the bus lines from being clamped to a permanent dominant level and thus from blocking all network communication.

The function of the TXD dominant time-out is illustrated in Figure 4-2. After a maximum allowable TXD dominant time (t_{DOM}) the transmitter of the transceiver will be disabled, thus releasing the bus lines to recessive again. The next dominant output drive is possible only after setting TXD to "HIGH" again. According to the CAN protocol a maximum of eleven successive dominant bits is allowed on TXD only (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum specified TXD dominant time-out ($t_{DOM\ MIN}$), this will limit the minimum suitable bit rate to 40kbit/s.

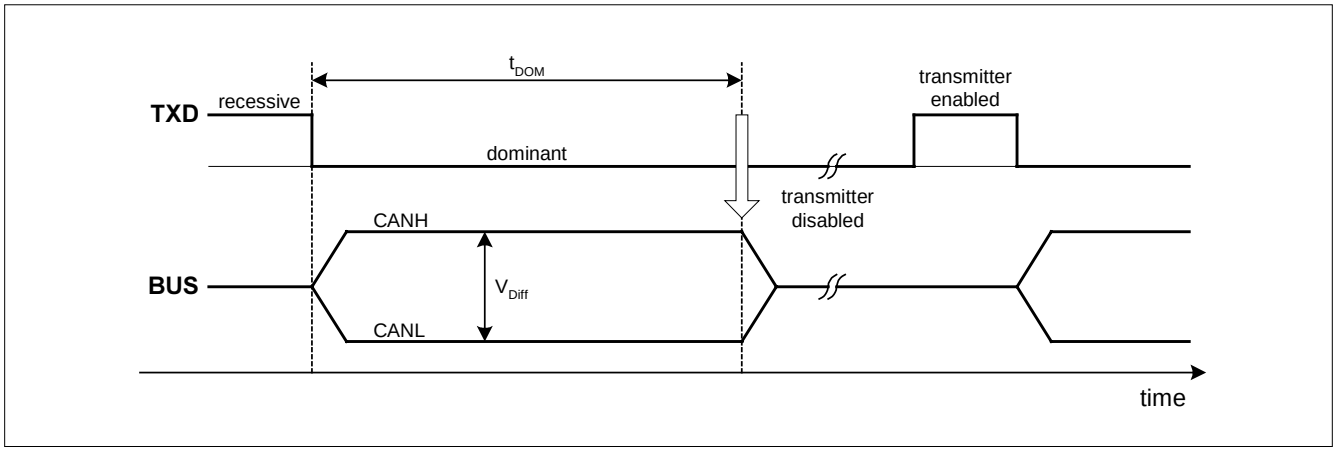

Figure 4-2: TXD dominant time-out feature

5. Hardware application

Besides the excellent behaviour of the TJA1040 itself, a careful system implementation dealing with termination, topology and external circuitry is very important in order to make optimum use of the transceivers advantages. This chapter presents a typical application example for the TJA1040 and application hints dealing with the split termination concept and external required circuitry for the TJA1040.

Figure 5-1 shows how to integrate the TJA1040 within a typical application. The application example assumes a 5V supplied host microcontroller. There is a dedicated 5V regulator supplying the TJA1040 transceiver and the microcontroller. Two capacitors are placed at the output of the voltage regulator for V_{CC} supply buffering purposes. The CAN-controller of the microcontroller is connected to the transceiver via TXD and RXD. The pin STB is connected to an I/O pin of the host microcontroller for operation mode control. The CAN bus lines are attached via the two bus terminals CANH and CANL. In-between matching capacitors are placed and a typical split termination is shown in order to improve EMC performance.

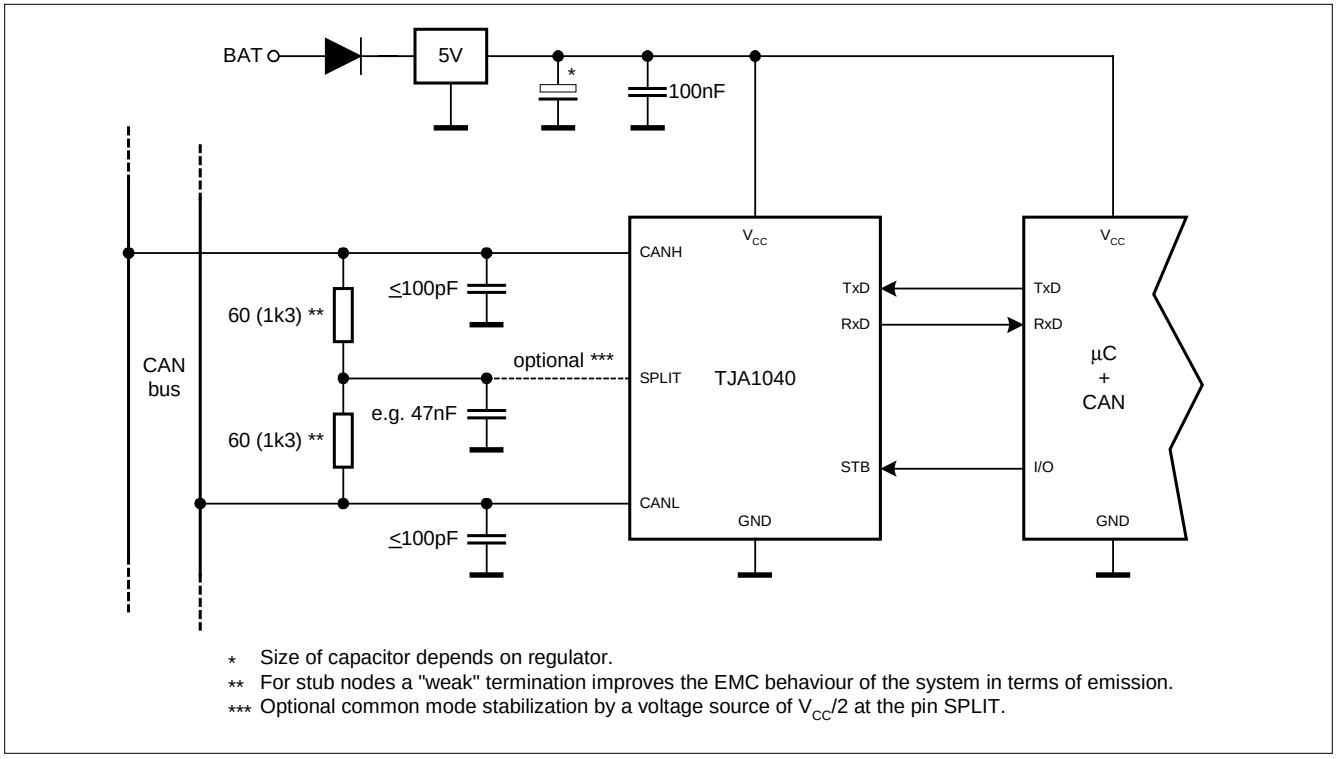

Figure 5-1: Typical application for the TJA1040 with a 5V microcontroller

5.1 Split termination concept

Practice has shown that effective reduction of electromagnetic emission can be achieved by a modified bus termination concept called “Split Termination”. In addition this concept contributes to higher immunity of the bus system. The split termination concept is illustrated in Figure 5-2. Basically each of the two termination resistors of the bus line end nodes is split into two resistors of equal value, i.e. two resistors of 60Ω instead of one resistor of 120Ω. It is common practice to include the termination within the ECU. As an option, stub nodes, which are connected to the bus via stubs, can be equipped with a similar split termination configuration. The resistor value for the stub nodes has to be chosen such that the busload of all the termination resistors stays within the ISO-specified range of 50Ω to 65Ω. Up to a number of 10 nodes (8 stub nodes and 2 bus end nodes) a typical resistor value is 1.3kΩ.

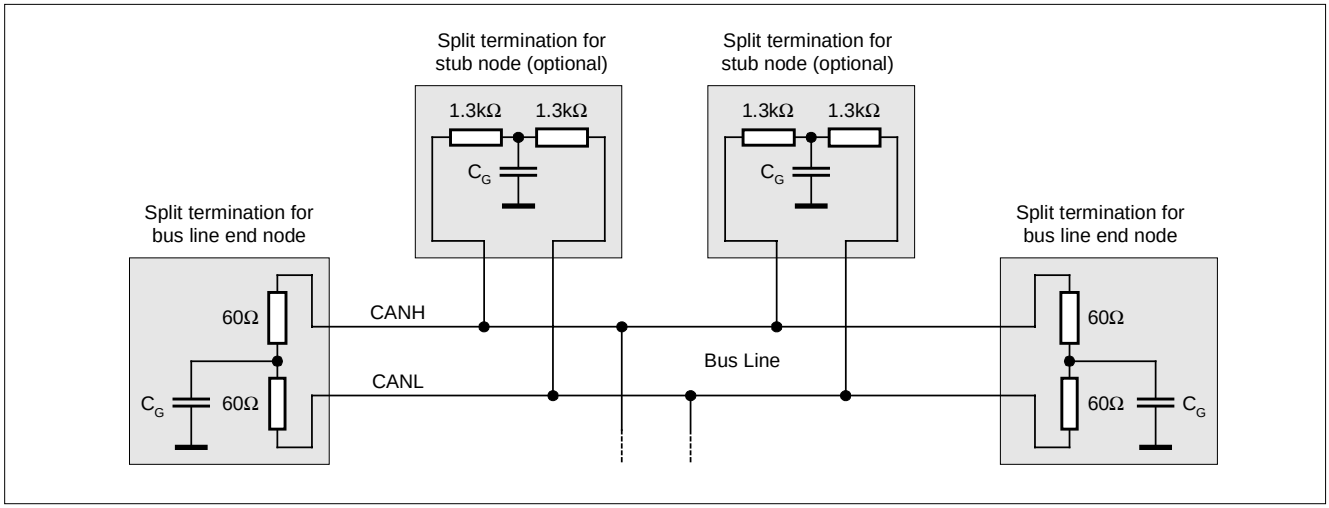

Figure 5-2: **Typical split termination concept**

The special characteristic of this approach is that the common mode signal is available at the center tap of the termination. This common mode signal is terminated to ground via a capacitor C_G of e.g. 4.7nF to 100nF. However, it is obvious that the capacitor should be connected to a “quiet” ground level. For example a separate ground lead to the ground pin of the module connector with lowest inductance is recommended, if termination is placed inside of bus nodes.

In order to make use of the TJA1040's very high output driver symmetry level, the symmetry of the two bus lines to reference ground becomes more and more important. Thus, the matching tolerance between the split termination resistors at each ECU has to be considered (recommended: ≤1%).

5.2 Optional circuitry at CANH and CANL

It is worth to notice that the EMC performance of the TJA1040 has been optimized for use of the split termination without a choke. Hence, it is highly recommended to implement the split termination. The excellent output stage symmetry allows going without chokes as shown by different emission measurements. If, however, the system performance is still not sufficient, there will be the option to use additional measures like common mode chokes, capacitors and ESD clamping diodes.

5.2.1 Common Mode Choke

A common mode choke provides high impedance for common mode signals and low impedance for differential signals. Due to this, common mode signals produced by RF noise and/or by non-perfect transceiver driver symmetry are damped significantly. Thus, common mode chokes help to reduce emission and to enhance immunity. Figure 5-3 shows how to combine a common mode choke with the split termination, capacitors and ESD clamping diodes.

Besides of the RF noise reduction the inductance of the choke may establish a resonant circuit together with pin capacitances. This can result in unwanted oscillations between the bus pins and the choke, both for differential and common mode signals. Oscillations of the differential signal can cause multiple switching of RXD.

Former transceiver products usually needed a common mode choke to fulfil the stringent emission and immunity requirements of the car manufacturers when using unshielded twisted-pair cable. The TJA1040 has the potential to build up in-vehicle bus systems without chokes. Whether chokes are needed finally depends on the specific system implementation like the wiring harness and the symmetry of the two bus lines (matching tolerances of resistors and capacitors).

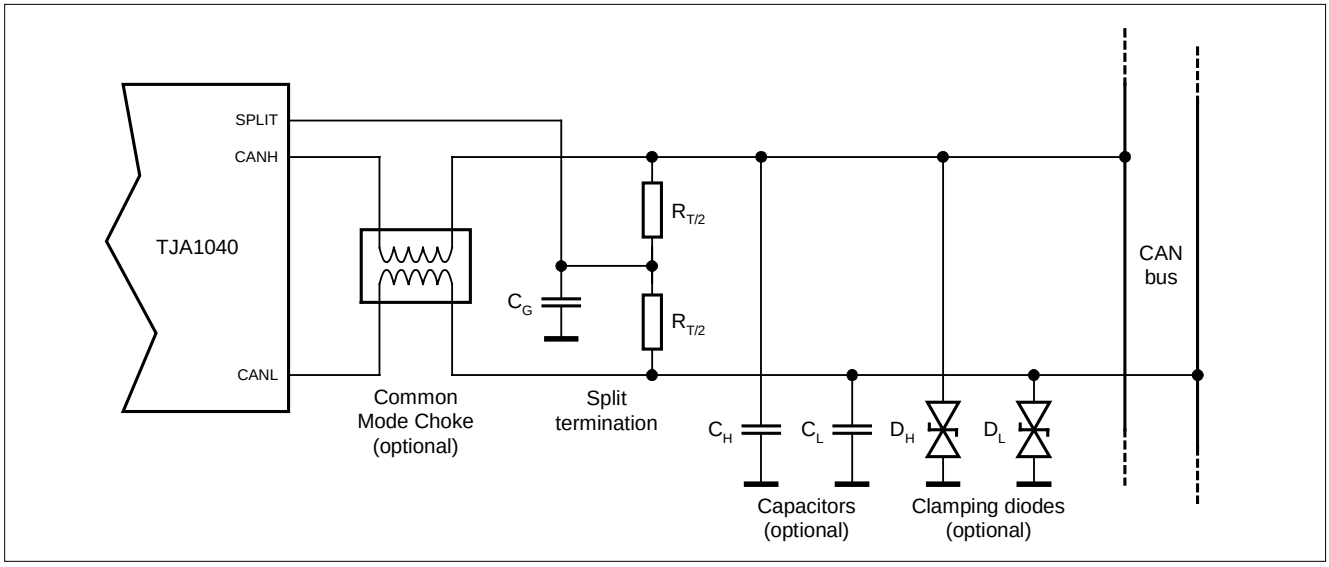

Figure 5-3: Optional circuitry at CANH and CANL

5.2.2 Capacitors

Matching capacitors (in pairs) at CANH and CANL to GND (C_H and C_L) are frequently used to enhance immunity against electromagnetic interference. Along with the impedance of corresponding noise sources (RF), capacitors at CANH and CANL to GND are forming a RC low-pass filter. Regarding immunity the capacitor value should be as large as possible in order to achieve a low corner frequency. On the other hand, the overall capacitive load and the impedance of the output stage establish a RC low-pass filter for the data signals. Thus the associated corner frequency must be well above the data transmission frequency. This results in a limit for the capacitor value depending on the number of nodes and the data transmission frequency. Notice that capacitors are increasing the signal loop delay due to reducing rise and fall times. Due to that, bit timing requirements, especially at 500kbit/s, call for a value of lower than 100pF (see also SAE J2284 and ISO11898). At a bit rate of 125kbit/s the capacitor value should not exceed 470pF. Typically, the capacitors are placed between the common mode choke (if applied at all) and the ESD clamping diodes as shown in Figure 5-3.

5.2.3 ESD protection

The TJA1040 is designed to withstand ESD pulses up to 6kV according to the human body model and thus typically does not need further external protection methods. Nevertheless, if much higher protection is required, external clamping circuits can be applied to the CANH and CANL line.

In Figure 5-3 the optional external ESD protection is realized with two clamping diode structures at CANH and CANL to GND (D_H and D_L). The clamping voltage of these suppressor diodes should be chosen above the maximum battery supply voltage of the system in order not to damage the diodes, if there is a short to battery on the bus lines. It is recommended to apply the ESD protection circuitry close to the connectors of the ECU as shown within Figure 5-3.

Figure 5-4 shows two alternative protection strategies. On the left side an optional circuit structure for ESD protection with three clamping diodes D_H, D_L and $D_{H/L}$ is shown. On the right side a proposal with two varistors R_H and R_L is given.

For both it has to be taken into account that the clamping diodes as well as the varistors provide a capacitance, which has to be added to the total capacitance of the bus connection. With a given maximum capacitance at CANH and CANL per node, the two capacitances C_H and C_L have to be adjusted in a way that the sum of the individual capacitances does not exceed the maximum allowable value.

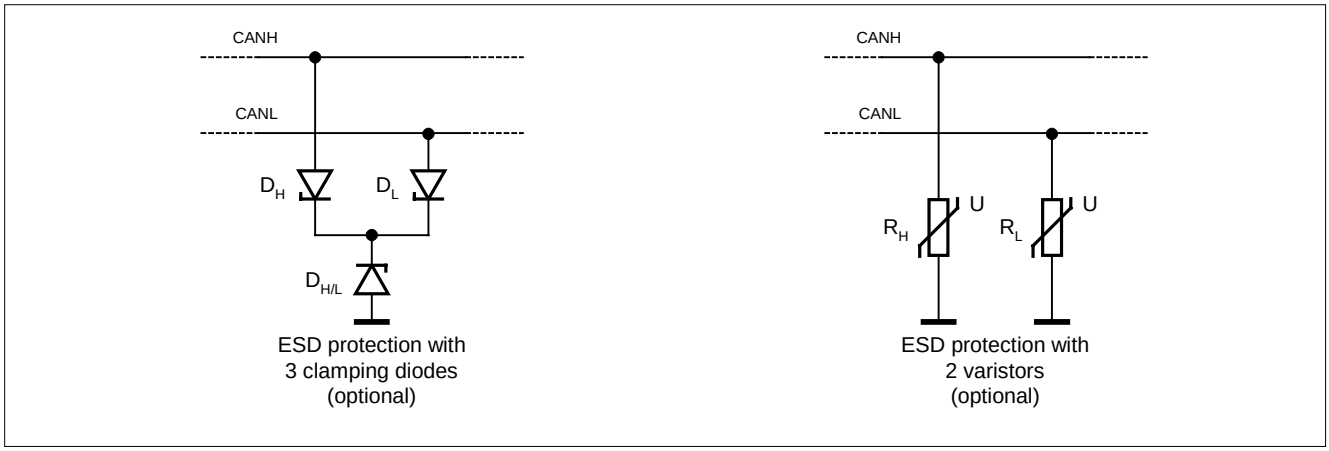

Figure 5-4: Alternative ESD protection circuits

5.3 Buffering at V_{CC}

The voltage supply via the pin V_{CC} provides the current needed for the transmitter and receiver of the TJA1040. The voltage regulator for the supply must be able to deliver a current of 71mA in average for the transceiver. Using a linear voltage regulator, it is recommended to stabilize the output voltage with a bypass capacitor of about 22µF. As illustrated in Figure 5-1 this type of capacitor should be connected at the output of the voltage regulator.

An additional capacitor in the range of 47nF to 100nF should be connected between V_{CC} and GND close to the transceiver. Its function is to buffer the V_{CC} supply voltage. For reliability reasons it might be useful to apply two capacitors in series connection between V_{CC} and GND. Thus, a single shorted capacitor cannot short-circuit the V_{CC} supply.

5.4 Optional circuitry at TXD and RXD

Depending on the used microcontroller and PCB layout, the digital signals at TXD and RXD during bit transitions might degrade the system EMC performance. Here a series resistor of about 1kΩ within the TXD and/or RXD line could be an option to reduce the electromagnetic emission of the system. Along with pin capacitance this would help to smooth the edges to some degree. For high bus speeds (≥500kbit/s) the additional delay within TXD and RXD has to be taken into account.

6. PIN FMEA

This chapter provides a FMEA (Failure Mode and Effects Analysis) for the typical failure situations, when dedicated pins of the TJA1040 are short-circuited to unexpected voltage levels like V_{BAT}, V_{CC}, GND or are simply be left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in Table 6-1.

Class	Effects
A	- Damage to transceiver - Bus may be affected
B	- No damage to transceiver - No bus communication possible
C	- No damage to transceiver - Bus communication possible - Corrupted node not able to communicate
D	- No damage to transceiver - Bus communication possible - Reduced functionality of transceiver

Table 6-1: Classification of failure effects

Table 6-2 and Table 6-3 show the FMEA matrix with the failure classifications and additional remarks on the further failure effects:

Pin	Short to V_{BAT} (12V … 40V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive; node eventually goes Bus-Off
(2) GND	C	Node is left unpowered	C	Transceiver is left unpowered
(3) V_{CC}	A	Limiting value exceeded	---	---
(4) RXD	A	Limiting value exceeded	C	RXD is clamped recessive and CAN controller expects an idle bus; node produces Error Frames on bus until Bus-Off is entered; communication continuously disturbed due to random communication trials of shorted node
(5) SPLIT	D	Bus charged to V_{BAT} - level; bit timing problem possible	D	Bus charged to V_{CC} - level; bit timing problem possible
(6) CANL	B	No bus communication	B	No bus communication
(7) CANH	D	Degradation of EMC; bit timing problem possible	D	Degradation of EMC; bit timing problem possible
(8) STB	A	Limiting value exceeded	C	Transceiver permanent in Standby Mode (transmitter disabled)

Table 6-2: FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; transmitter disabled; node eventually goes Bus-Off	C	TXD clamped recessive; node eventually goes Bus-Off
(2) GND	---	---	C	Transceiver is left unpowered and behaves passive to the bus lines
(3) V_{CC}	C	Transceiver is left unpowered and behaves passive to the bus lines	C	Transceiver is left unpowered; no V_{CC} reverse supply from µC to transceiver
(4) RXD	C	RXD clamped dominant	C	Node may produce Error Frames on bus until Bus-Off is entered
(5) SPLIT	D	Bus discharged to GND - level; bit timing problem possible	D	No DC common mode stabilization
(6) CANL	D	Degradation of EMC; bit timing problem possible	C	Receiving from bus possible only, if there is no termination resistor within this interrupted bus segment present; transmitting across the interruption is not possible
(7) CANH	B	No bus communication	C	Receiving from bus possible only, if there is no termination resistor within this interrupted bus segment present; transmitting across the interruption is not possible
(8) STB	D	Transceiver permanent in Normal Mode	C	Transceiver permanent in Standby Mode (transmitter disabled)

Table 6-3: FMEA matrix for pin short-circuits to GND and open pins

7. Bus network aspects

This chapter deals with items like the maximum number of nodes, the maximum bus line length and topology aspects. Especially the topology appears to have a significant influence on the system performance.

7.1 Maximum Number of nodes

The number of nodes, which can be connected to a bus, depends on the minimum load resistance a transceiver is able to drive. The TJA1040 transceiver provides an output drive capability down to a minimum load of $R_{L,min}$ = 45Ω for V_{CC} > 4.75V. The overall busload is defined by the termination resistance R_T, the bus line resistance R_W and the transceiver's differential input resistance R_{diff}. The DC circuit model of a bus system is shown in Figure 7-1. For worst case consideration the bus line resistance R_W is considered to be zero. This leads to the following relations for calculating the maximum number of nodes:

$$\frac{R_{T.\min} \times R_{diff.\min}}{n_{\max} \times R_{T.\min} + 2R_{diff.\min}} > R_{L.\min} \Rightarrow n_{\max} < R_{diff.\min} \times \left(\frac{1}{R_{L.\min}} - \frac{2}{R_{T.\min}} \right)$$

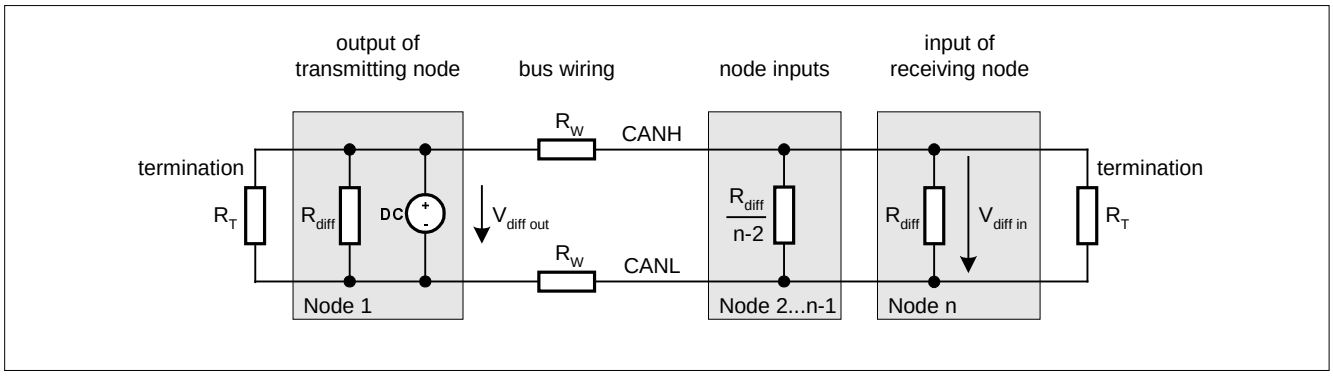

Figure 7-1: **DC circuit model for a bus system according to ISO11898**

Table 7-1 gives the maximum number of nodes for two different termination resistances. Notice that connecting a large number of nodes requires relatively large termination resistances.

Transceiver	$R_{diff,min}$ (kΩ)	$R_{L,min}$ (Ω)	Nodes (maximum) ($R_{T,min}$=118Ω)	Nodes (maximum) ($R_{T,min}$=130Ω)
TJA1040 TJA1041 TJA1050	25	45 @ V_{CC}=4.75V	131	170
C250 C251	20	45 @ V_{CC}=4.9V	105	136

Table 7-1: **Maximum number of nodes** (see datasheets for $R_{diff,min}$ & $R_{L,min}$)

7.2 Maximum Bus Line Length

The maximum achievable bus line length in a CAN network is determined essentially by the following physical effects:

1. The loop delays of the connected bus nodes (CAN controller, transceiver etc.) and the delay of the bus line.
2. The relative oscillator tolerance between nodes.

3. The signal amplitude drop due to the series resistance of the bus cable and the input resistance of bus nodes (for a detailed description refer to [10]).

Effects 1 and 2 result in a value for the maximum bus line length with respect to the CAN bit timing [9]. Effect 3, on the other hand, results in a value with respect to the output signal drop along the bus line. The minimum of the two values has to be taken as the actual maximum allowable bus line length. As the signal drop is only significant for very long lengths, effect 3 can often be neglected for high data rates.

Specification	Data Rate		
	125kbit/s (BT tol. = +/- 1.25%)	**250kbit/s** (BT tol. = +/- 0.75%)	**500kbit/s** (BT tol. = +/- 0.5%)
SAE J2284	50m	50m	30m
TJA1040	80m	80m	40m

Table 7-2: **Maximum bus line length for some standards and the TJA1040**
(BT tol. = Bit Time Tolerance)

Table 7-2 gives the maximum bus line length for the bit rates 125kbit/s, 250kbit/s and 500kbit/s, along with values specified in the SAE J2284 [3] standard associated to CAN. The calculation is based on effects 1 and 2 assuming a minimum propagation delay between any two nodes of 200ns and a maximum bus signal delay of 8ns/m. Notice that the stated values apply only for a well-terminated linear topology. Bad signal quality because of inadequate termination can lower the maximum allowable bus line length.

7.3 Topology Aspects

The topology describes the wiring harness structure. Typical structures are linear, star- or multistar-like. In automotive, shielded or unshielded twisted pair cable usually functions as a transmission line. Transmission lines are generally characterized by the length-related resistance R_{Length}, the specific line delay t_{delay} and the characteristic line impedance Z. Table 7-3 shows the physical media parameters specified in the ISO11898 and SAE J2284 standard. Notice that SAE J2284 specifies the twist rate r_{twist} in addition.

Parameter	Notation	Unit	ISO 11898			SAE J2284		
			Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
Impedance	Z	Ω	95	120	140	108	120	132
Length-related resistance	R_{Length}	mΩ/m	-	70	-	-	70	-
Specific line delay	t_{delay}	ns/m	-	5	-	-	5.5	-
Twist rate	r_{twist}	twist/m	-	-	-	33	-	50

Table 7-3: **Physical media parameters of a pair of wires (shielded or unshielded)**

7.3.1 Ringing due to Signal Reflections

Transmission lines must be terminated with the characteristic line impedance, otherwise signal reflections will occur on the bus causing significant ringing. The topology has to be chosen such that reflections will be minimized. Often the topology is a trade-off between reflections and wiring constraints.

CAN is well prepared to deal with reflection ringing due to some useful protocol features:

1. Only recessive to dominant transitions are used for resynchronization.

2. Resynchronization is allowed only once between the sample points of two bits and only, if the previous bit was sampled and processed with recessive value.
3. The sample point is programmable to be close to the end of the bit time.

7.3.2 Linear Topology

The CAN High-Speed standard ISO11898 defines a single line structure as network topology. The bus line is terminated at both ends with a single termination resistor. The nodes are connected via not terminated drop cables or stubs to the bus. In order to keep the ringing duration short compared to the bit time, the stub length should be as short as possible. For example the ISO11898 standard limits the stub length to 0.3m at 1Mbit/s. The corresponding SAE standard, J2284-500, recommends keeping the stub length below 1m. To minimize standing waves, ECUs should not be placed equally spaced on the network and cable tail lengths should not all be the same [3]. Table 7-4 along with Figure 7-2 illustrates the topology requirements of the SAE J2284-500 standard. At lower bit rates the maximum distance between any two ECUs as well as the ECU cable stub lengths may become longer.

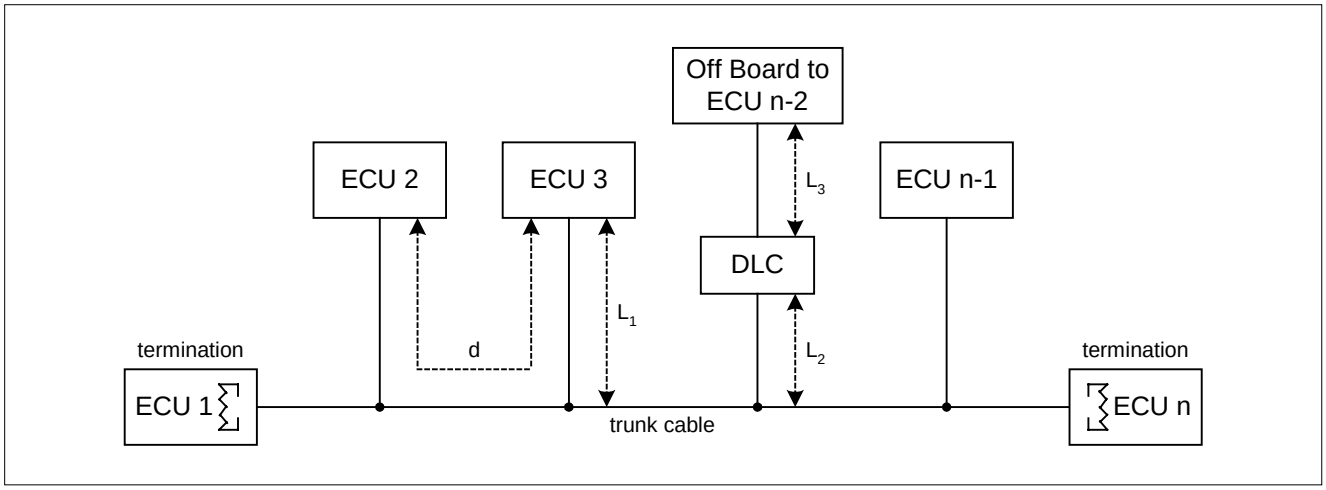

Figure 7-2: **Topology requirements of SAE J2284**

In practice some deviation from that stringent topology proposals might be necessary, because longer stub lengths are needed. Essentially the maximum allowable stub length depends on the bit timing parameters, the trunk cable length and the accumulated drop cable length. For a rule of thumb calculation of the maximum allowable stub length refer to [10].

The star topology is neither covered by ISO11898 nor by SAE J2284. However, it is sometimes used in automotive applications to overcome wiring constraints within the car. Generally, the signal integrity suffers from a star topology compared to a linear topology. It is recommended to prove the feasibility of a specific topology in each case by simulations or measurements on a system set-up.

Parameter	Symbol	Unit	Min.	Nom.	Max.
ECU cable stub length	L1	m	0	-	1
In-vehicle DLC cable stub length	L2	m	0	-	1
Off board DLC cable stub length	L3	m	0	-	5
Distance between any two ECUs	d	m	0.1	-	30

Table 7-4: **ECU topology requirements of SAE J2284-500**

8. Interoperability

Interoperability of the CAN High-Speed Transceivers C250, C251, TJA1040, TJA1041 and TJA1050 (see also Appendix 11.1) is guaranteed due to their compatibility to the ISO11898 standard. They are able to work together in the same bus network.

There are some issues related to different bus biasing behaviour during low-power operation, which are considered in this chapter. Table 8-1 shows the bus biasing in the different operation modes as well as in unpowered condition. Whenever there is a difference in the bus biasing, a steady DC compensation current will flow within the system. The common mode input resistance mainly defines the amount of this compensation current. This is shown in Figure 8-1 for a bus in recessive state including TJA1040 and TJA1041 nodes.

Transceiver	Operation Mode	Bus Bias
TJA1040	Normal	$V_{CC}/2$
	Standby	weak GND
	Unpowered	floating
TJA1041	Normal, Pwon/Listen-Only	$V_{CC}/2$
	Standby, Sleep, Go-to-Sleep, Unpowered	weak GND
TJA1050	Normal, Silent	$V_{CC}/2$
	Unpowered	weak GND
C250/C251	Normal, Standby	$V_{CC}/2$
	Unpowered	GND

Table 8-1: Bus biasing of Philips Transceivers depending on operation mode

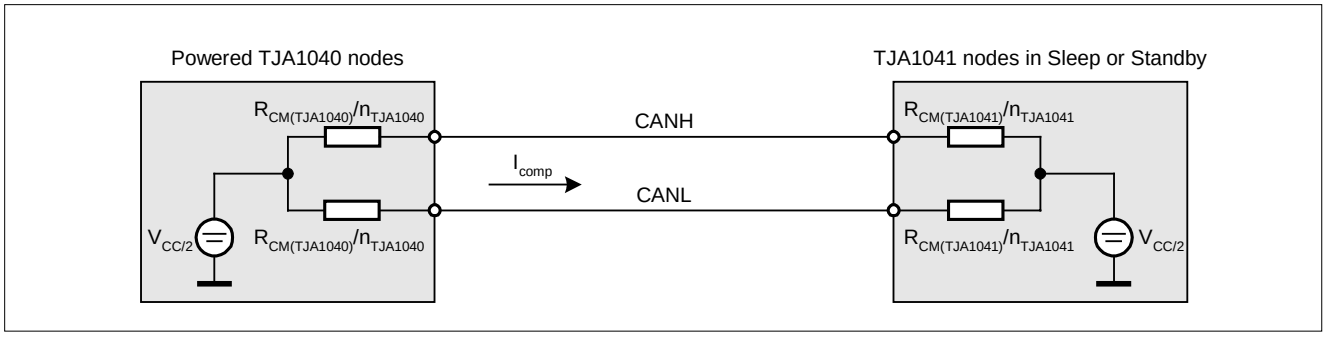

Figure 8-1: Equivalent bus circuit for a mixed system of TJA1040 nodes in Normal Mode and TJA1041 nodes in Standby/Sleep Mode

Due to the large common mode input resistance CAN communication is not affected in case parts of the network are still within low-power mode, while other nodes have already started communication. However, degradation of the emission performance is expected.

The following formula allows calculation of the whole biasing compensation current in a mixed system of TJA1040 and TJA1041 nodes.

$$I_{comp,\max} = \frac{Vcc/2}{R_{CM}(TJA1040)/2n_{TJA1040} + R_{CM}(TJA1041)/2n_{TJA1041}}$$

with $n_{TJA1040}$: number of nodes of powered TJA1040

$n_{TJA1041}$: number of nodes of TJA1041 in Standby/Sleep Mode

$R_{CM}(TJA1040)$ =15k: min. common mode input resistance of TJA1040 at pin CANH/L

$R_{CM}(TJA1041)$ =15k: min. common mode input resistance of TJA1041 at pin CANH/L

Transceiver		TJA1040		
		Normal	Standby	Unpowered
TJA1041	Normal	---	X	---
	Pwon/Listen-Only	---	X	---
	Standby	X	---	---
	Sleep	X	---	---
	Goto-Sleep	X	---	---
	Unpowered	X	---	---
TJA1050	Normal	---	X	---
	Silent	---	X	---
	Unpowered	X	---	---
C250/C251	Normal	---	X	---
	Standby	---	X	---
	Unpowered	X	---	---

Table 8-2: Conditions leading to DC compensation current

X : DC compensation current

---: no DC compensation current

Table 8-2 identifies the conditions leading to different bus biasing and thus DC compensation current when different CAN High-Speed Transceivers are working together in the same bus network. The perfect passive behaviour of the TJA1040 when unpowered is clear recognisable in Table 8-2 since an unpowered TJA1040 node never leads to a DC compensation current.

8.1 TJA1040 mixed with TJA1041 nodes

In a mixed system of TJA1040 and TJA1041 nodes, it is not expected to have situations of different bus biasing. In the low-power modes both the TJA1040 and TJA1041 show a weak termination to GND. Thus when the bus is in power-down with all nodes either in Standby or Sleep Mode, there will be no DC compensation current. During normal CAN operation, when all nodes are in Normal (High-Speed) or Pwon/Listen-Only Mode for diagnosis features, the bus is collectively biased to $V_{CC}/2$. There will be no DC compensation current.

8.2 TJA1040 mixed with TJA1050 or C250/C251 nodes

Table 8-2 reveals also that some compensation current is flowing in case TJA1040 nodes are in Normal Mode, while other TJA1050 or C250/C251 nodes are left unpowered. Moreover, compensation current occurs when TJA1040 nodes are in Standby Mode, while other TJA1050 or C250/C251 nodes are kept powered in any operation mode. However, the compensation current is negligible compared to the current saving due to the very low standby supply current of the TJA1040. So, upgrading existing C250/C251 ECUs with the TJA1040 will always improve the overall current budget of the system, even if there are some C250/C251 nodes left in the vehicle.

9. Upgrading hints

This chapter describes all items to be taken into account, when an existing application using the C250/C251 transceivers should be upgraded towards the TJA1040. In Figure 9-1 and Figure 9-2 typical application circuits for the C250/C251 and TJA1040, respectively, are shown.

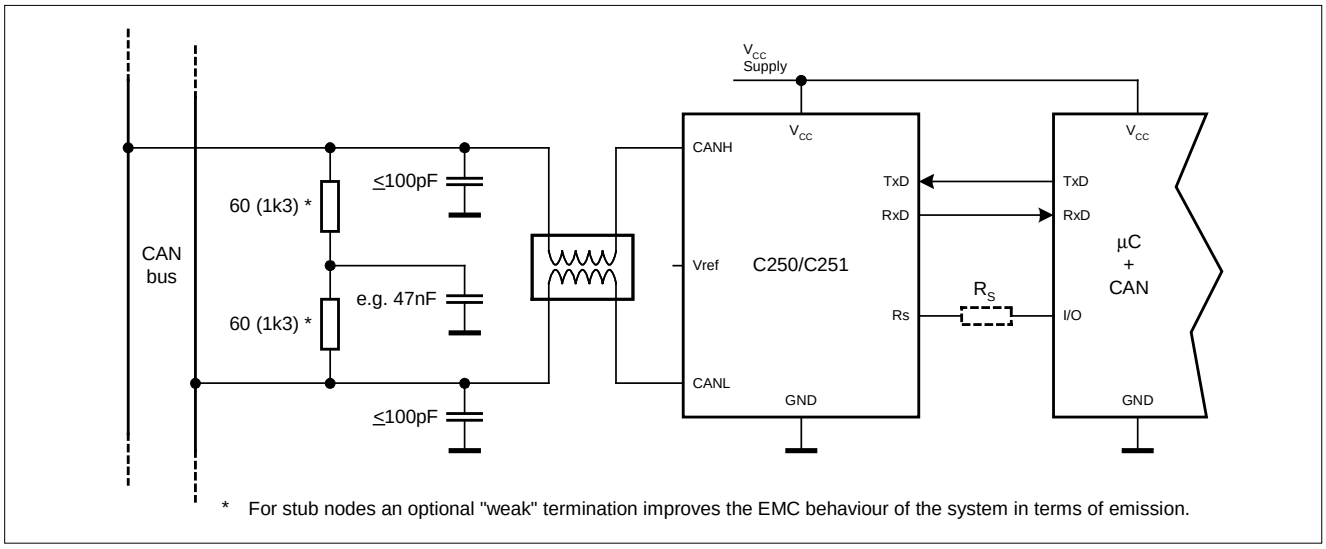

Figure 9-1: Typical application circuit for the C250/C251

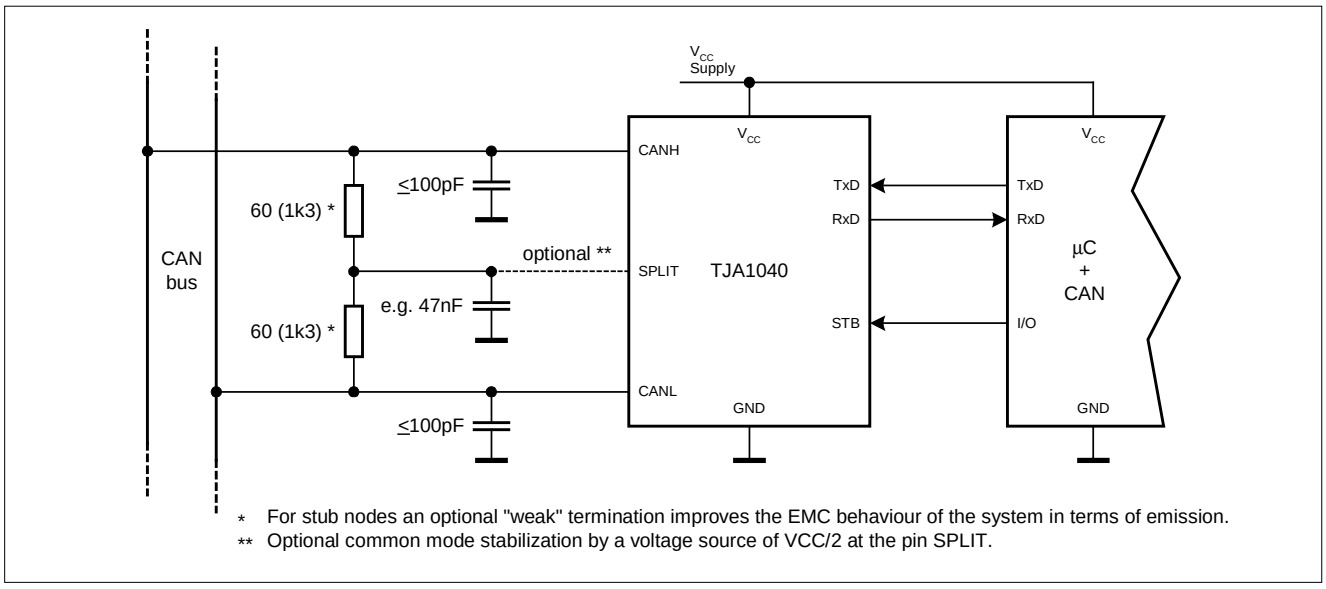

Figure 9-2: Typical application circuit for the TJA1040

9.1.1 Hardware Check-List C250/C251 → TJA1040

Comparing the application circuits in Figure 9-1 and Figure 9-2, the following items have to be checked when replacing the C250/C251 by the TJA1040:

- If the pin SPLIT should be used for DC stabilization of the common mode voltage, the pin SPLIT (corresponds to pin Vref of C250/C251) is connected optionally to the center tap of the split termination. The pin SPLIT can simply be left open, if not used.
- If the mode control pin 8 of the C250/C251 was applied with a slope control resistor R_S for slope control, this resistor has to be removed. The corresponding pin of the TJA1040 (pin STB) should be directly connected to an output port of the microcontroller. There is the same polarity vs. function of this signal and thus, no need for a software modification.
- The TJA1040 does not necessarily need a common mode choke. The split termination is highly recommended as it ensures lowest emission, especially in the AM-band.

10. References

[1] Data Sheet TJA1040, High-Speed CAN transceiver, Philips Semiconductors, 2003 Feb 19

[2] Road Vehicles - Interchange of Digital Information - Controller Area Network (CAN) for high-speed communication, ISO11898, 1993

Road Vehicles - Controller Area Network (CAN) - Part 2: High-speed medium access unit, ISO11898-2, DIS 2002

[3] High Speed CAN (HSC) for Vehicle Applications at 500kbps, SAE J2284, 1999

[4] Data Sheet TJA1050, High Speed CAN transceiver, Philips Semiconductors, 2002 May 16

[5] Data Sheet PCA82C250, CAN controller interface, Philips Semiconductors, 2000 Jan 13

[6] Data Sheet PCA82C251, CAN controller interface, Philips Semiconductors, 2000 Jan 13

[7] Data Sheet TJA1041, High-Speed CAN transceiver, Philips Semiconductors, 2003 Feb 13

[8] SAE Conference Paper 950298, EMC Measures for Class C Communication Systems using Unshielded Cable, Lütjens/Eisele 1995

[9] Application Note AN97046, Determination of Bit Timing Parameters for the CAN Controller SJA1000, Philips Semiconductors, 1997

[10] Application Note AN96116, PCA82C250/251 CAN Transceiver, Philips Semiconductors, 1996

11. Appendix

11.1 Comparison of C250/C251, TJA1040, TJA1041 and TJA1050

Table 11-1 lists the main differences between the C250/C251, TJA1040, TJA1041 and TJA1050 from an application point of view.

Feature	C250	C251	TJA1040	TJA1041	TJA1050
V_{CC} voltage range	4.5 - 5.5V	4.5 - 5.5V	4.75 - 5.25V	4.75 - 5.25V	4.75 - 5.25V
Max. DC voltage at bus pins	-8V…+18V	-36V…+36V	-27V…+40V	-27V…+40V	-27V…+40V
Loop Delay	(R_S=0) 190ns (R_S=24k) 320ns	(R_S=0) 190ns	255ns	255ns	250ns
Standby Mode current consumption (remote wake-up)	< 170µA	< 275µA	< 15µA	< 10µA at V_{CC} < 30µA at BAT	Not supported
Sleep Mode current consumption (remote wake-up)	Not supported	Not supported	Not supported	< 30µA at BAT	Not supported
Slope Control	Variable	Variable	Fixed, EMC optimized	Fixed, EMC optimized	Fixed, EMC optimized
Passive behaviour (Leakage current of bus pins; V_{CC}=0V)	< 1000µA ($V_{CANH/L}$=7V)	< 2000µA ($V_{CANH/L}$=7V)	0µA ($V_{CANH/L}$=5V)	< 250µA ($V_{CANH/L}$=5V)	< 250µA ($V_{CANH/L}$=5V)
Common mode stabilization (SPLIT Pin)	No	No	Yes	Yes	No
Bus failure diagnosis	No	No	No	Yes	No
System Fail-Safe Features	No	No	TXD time-out; no reverse currents	TXD time-out; RXD clamping; V_{CC} clamping; no reverse currents	TXD time-out; no reverse currents
3V Microcontroller support	No	No	Yes, 5V tolerant RXD input at µC needed	Yes	Yes, 5V tolerant RXD input at µC needed
Power-on detection (first battery connection)	No	No	No	Yes	No

Table 11-1: Main differences between C250/C251, TJA1040, TJA1041 and TJA1050

Figure 11-1 shows the pinning of the C250/C251, TJA1040, TJA1041 and TJA1050. Apart from renaming two pins the pinning of the SO8 package transceivers is identical. Accordingly the upper part of the SO14 pinning of the TJA1041 is compatible to the SO8 pinning of the other transceiver products.

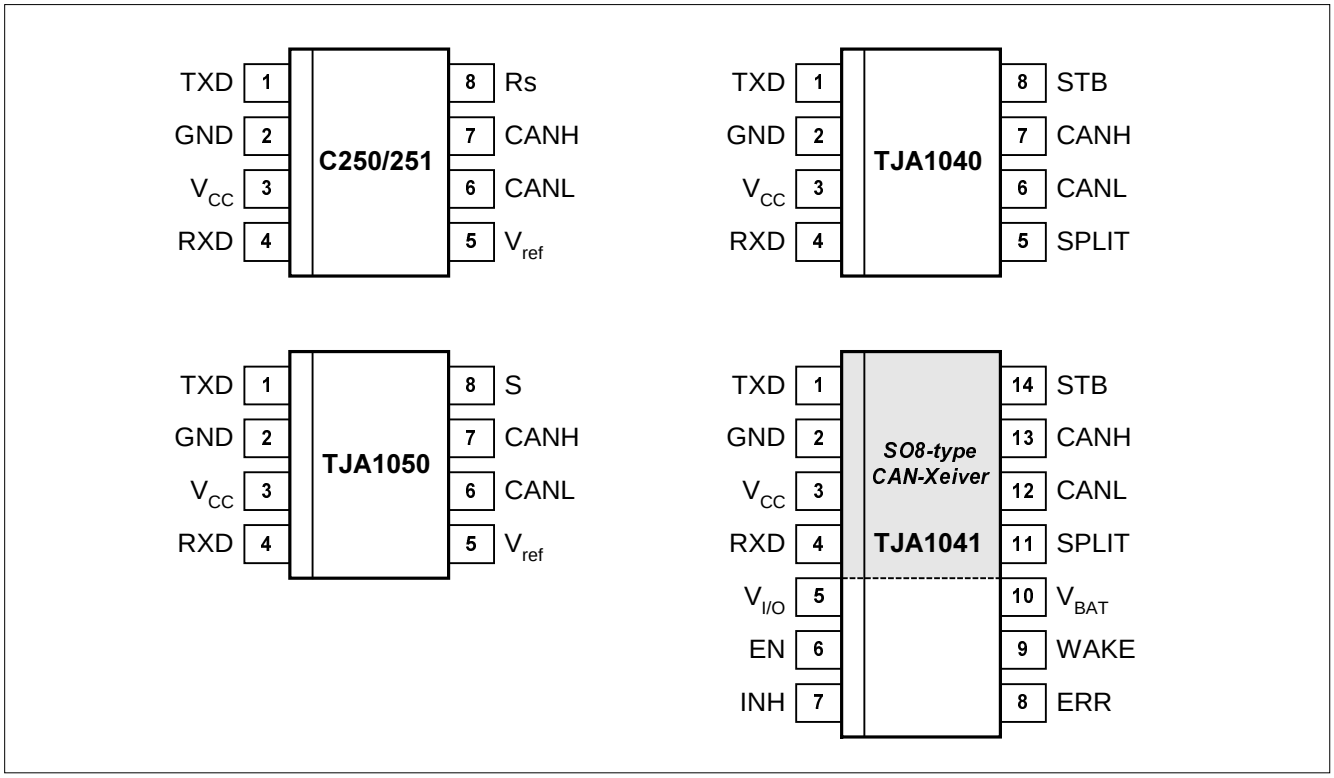

Figure 11-1: Pinning of the C250/C251, TJA1040, TJA1050 and TJA1041

11.2 Glossary

Abbreviation	Description
CAN	Controller Area Network
Clamp-15	ECU architecture, Battery supply line after the ignition key, module is temporarily supplied by the battery only (ignition key on)
Clamp-30	ECU architecture, direct battery supply line before the ignition key, module is permanently supplied by the battery
ECU	Electronic Control Unit
EMC	Electro Magnetic Compatibility
EME	Electro Magnetic Emission
EMI	Electro Magnetic Immunity
FMEA	Failure Mode and Effects Analysis
SOI	Silicon on Insulator

Table 11-2: Abbreviations